

**24N50**

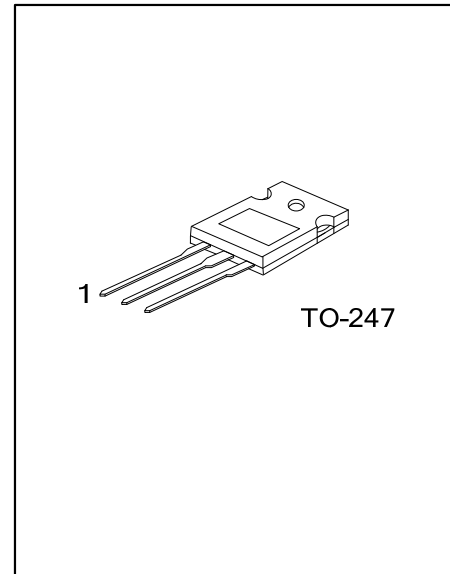
Preliminary

Power MOSFET**24 Amps, 500 Volts
N-CHANNEL POWER MOSFET**

■ DESCRIPTION

The UTC **24N50** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

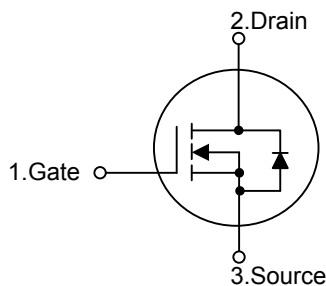
The UTC **24N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.



■ FEATURES

- * 24A, 500V, $R_{DS(ON)}=0.2\Omega$ @ $V_{GS}=10V$
- * High Switching Speed
- * 100% Avalanche Tested

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
24N50L-T47-T	24N50G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

24N50L-T47-T (1) Packing Type (2) Package Type (3) Lead Free		(1) T: Tube (2) T47: TO-247 (3) G: Halogen Free, L: Lead Free
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■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^{\circ}\text{C}$)	I_D	24 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	96 (Note 2)	A
Avalanche Current (Note 3)		I_{AR}	24	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	1100	mJ
	Repetitive (Note 5)	E_{AR}	29	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	15	V/ns
Power Dissipation	$T_C=25^{\circ}\text{C}$	P_D	290	W
	Derate above 25°C		2.33	W/ $^{\circ}\text{C}$
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^{\circ}\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Drain current limited by maximum junction temperature

3. Repetitive Rating: Pulse width limited by maximum junction temperature

4. $L = 3.4\text{mH}$, $I_{AS} = 24\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

5. $I_{SD} \leq 24\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	40	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.43	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

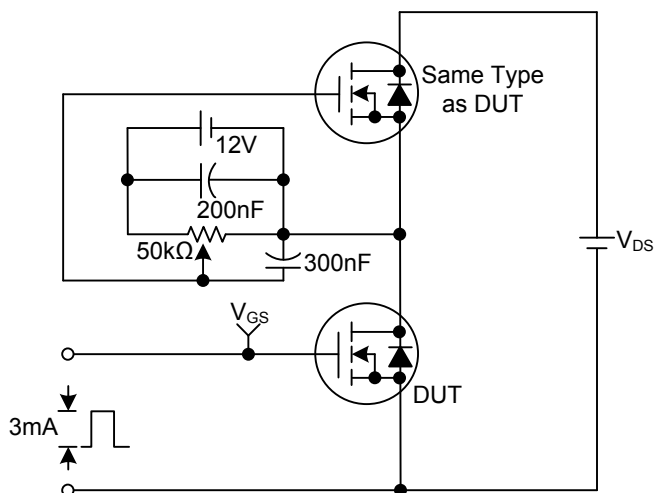
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	500			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =500V, V _{GS} =0V			1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =12A			0.2	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		3500	4500	pF
Output Capacitance		C _{OSS}			520	670	pF
Reverse Transfer Capacitance		C _{RSS}			55	70	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{GS} =10V, V _{DS} =400V, I _D =24A (Note 6, 7)		90	120	nC
Gate to Source Charge		Q _{GS}			23		nC
Gate to Drain Charge		Q _{GD}			52		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =250V, I _D =24A, R _G =25Ω (Note 6, 7)		80	170	ns
Rise Time		t _R			250	500	ns
Turn-OFF Delay Time		t _{D(OFF)}			200	400	ns
Fall-Time		t _F			155	320	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				24	A
Maximum Body-Diode Pulsed Current		I _{SM}				96	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =24A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{RR}	I _S =24A, V _{GS} =0V, dI _F /dt=100A/μs		250		ns
Body Diode Reverse Recovery Charge		Q _{RR}	(Note 6)		1.1		μC

Notes: 6. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

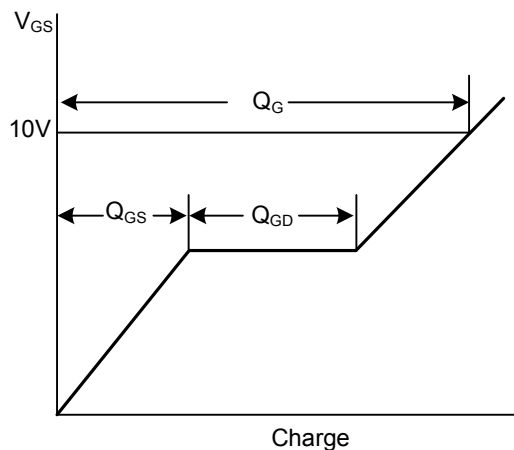
7. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

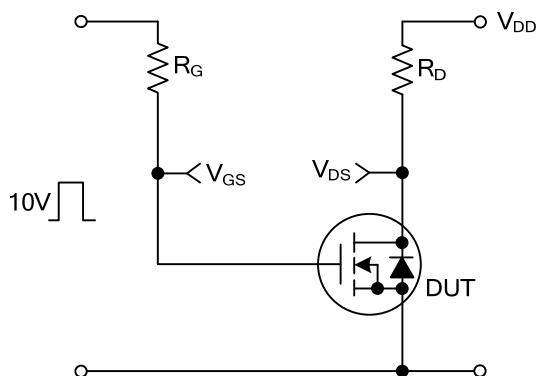
Gate Charge Test Circuit



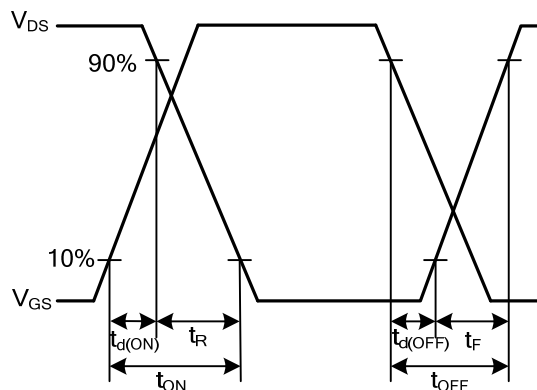
Gate Charge Waveforms



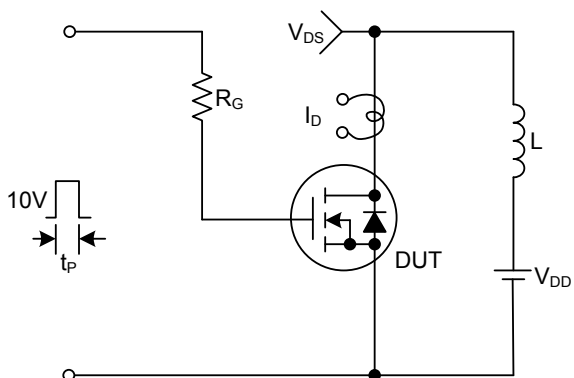
Resistive Switching Test Circuit



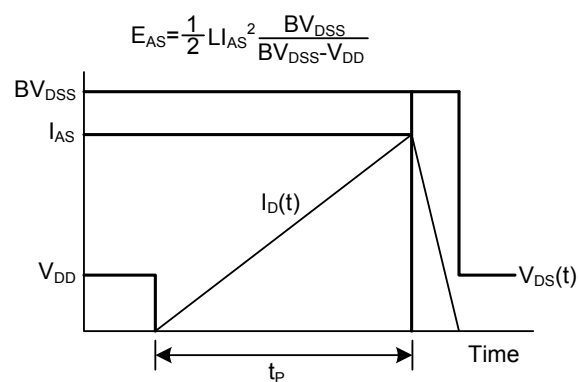
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit

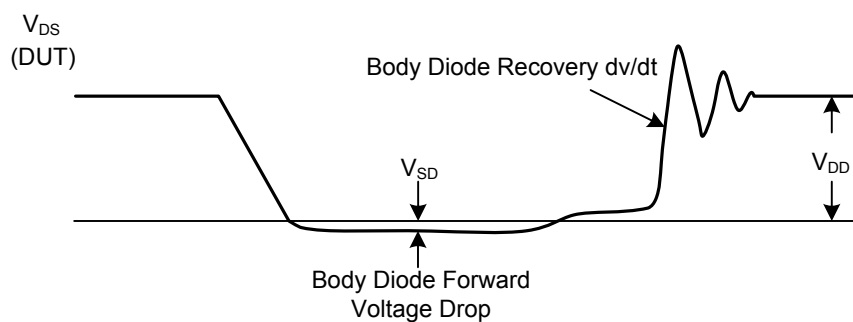
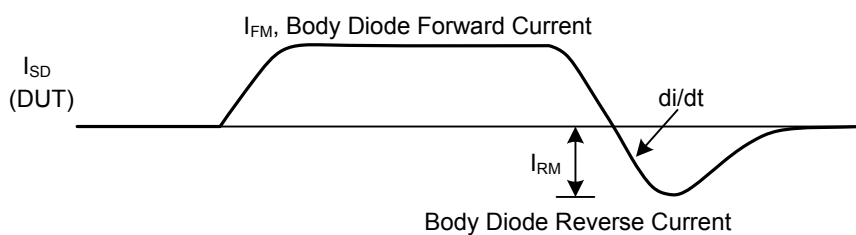
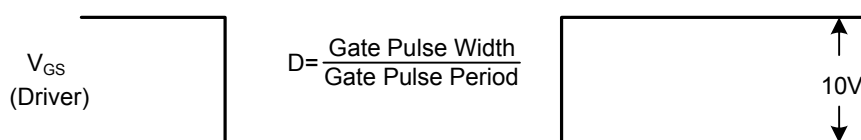
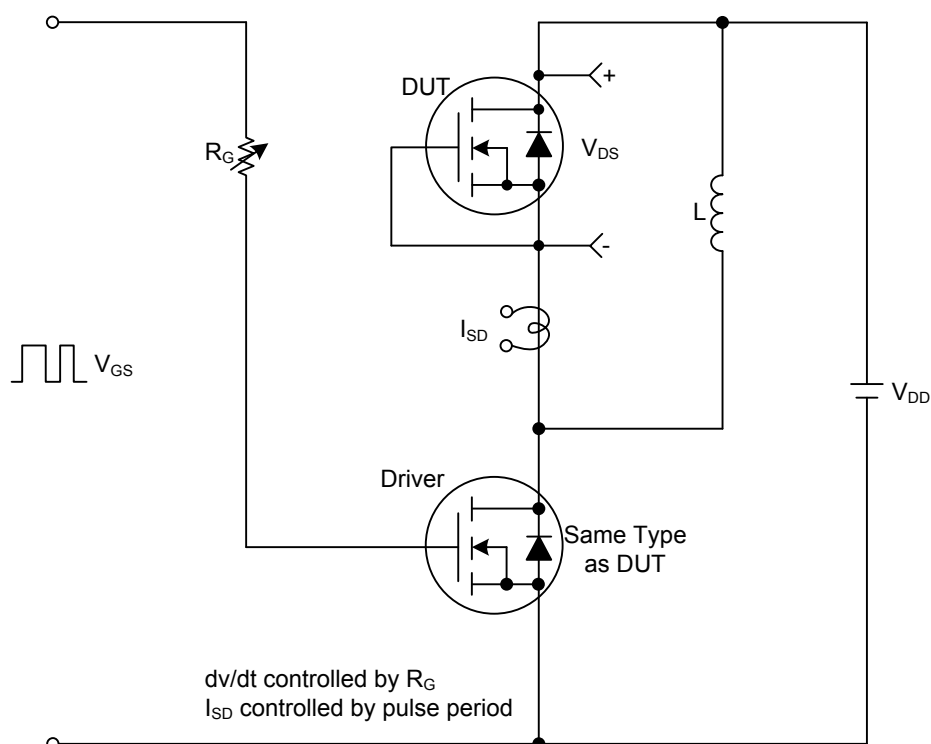


Unclamped Inductive Switching Waveforms



■ TEST CIRCUITS AND WAVEFORMS(Cont.)

Peak Diode Recovery dv/dt Test Circuit & Waveforms



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