

Silicon NPN Power Transistors

2SC1454

DESCRIPTION

- With TO-3 package
- High breakdown voltage: $V_{CE0}=250V(\text{min})$

APPLICATIONS

- For use in low frequency power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

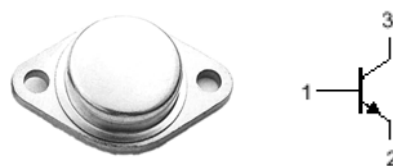


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a=^{\circ}\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	300	V
V_{CEO}	Collector-emitter voltage	Open base	250	V
V_{EBO}	Emitter-base voltage	Open collector	7	V
I_C	Collector current		4	A
P_C	Collector power dissipation	$T_C=25^{\circ}\text{C}$	50	W
T_j	Junction temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		-55~150	$^{\circ}\text{C}$

Silicon NPN Power Transistors**2SC1454****CHARACTERISTICS**T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =25mA ; I _B =0	250			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =3A; I _B =0.3A			1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =3A; I _B =0.3A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =300V; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =7V; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	20			
f _T	Transition frequency	I _C =0.5A ; V _{CE} =12V		10		MHz

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PACKAGE OUTLINE

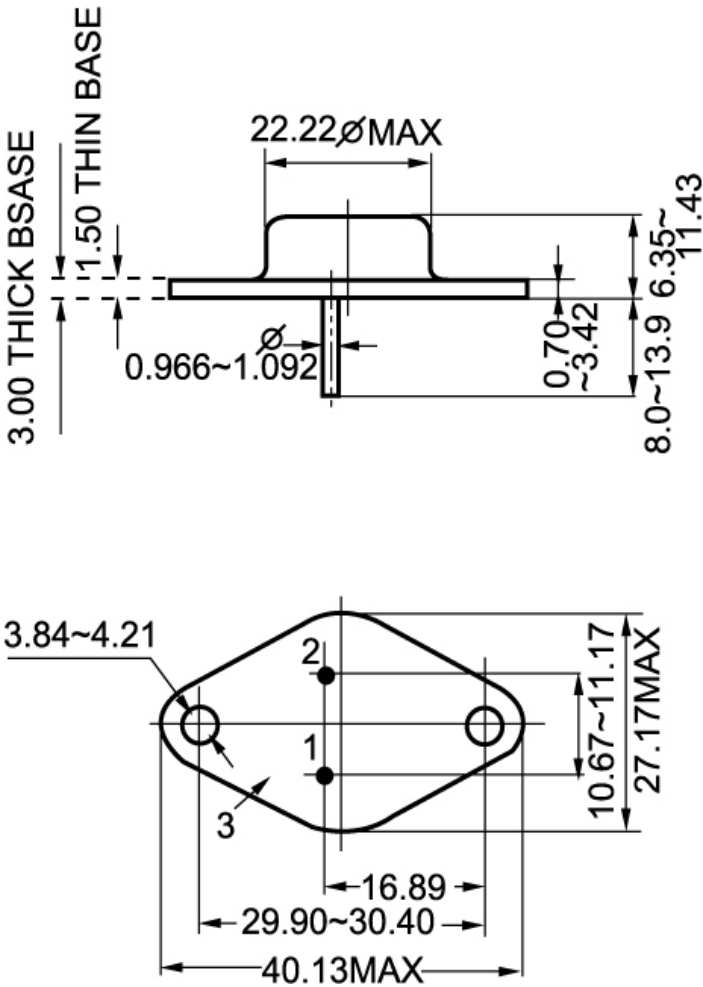


Fig.2 outline dimensions (unindicated tolerance: ±0.1mm)