

256-BIT TTL RAM (256 × 1)**54/74LS301 (O.C.)****DESCRIPTION**

The 54/74LS301 is a Read/Write memory array which features an open collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write ($\overline{D}_O$ terminal "H") permits $\overline{D}_O$ and $\overline{D}_{IN}$ terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

The 54/74LS301 is available in both the commercial temperature range (0°C to

+ 75°C) and the military temperature range (– 55°C to + 125°C). They are specified as: N74LS301F or N for the commercial temperature range, and S54LS301F, G, or W for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- Address access time:
N74LS301: 40ns max
S54LS301: 70ns max
- Write cycle time:
N74LS301: 25ns max
S54LS301: 60ns max

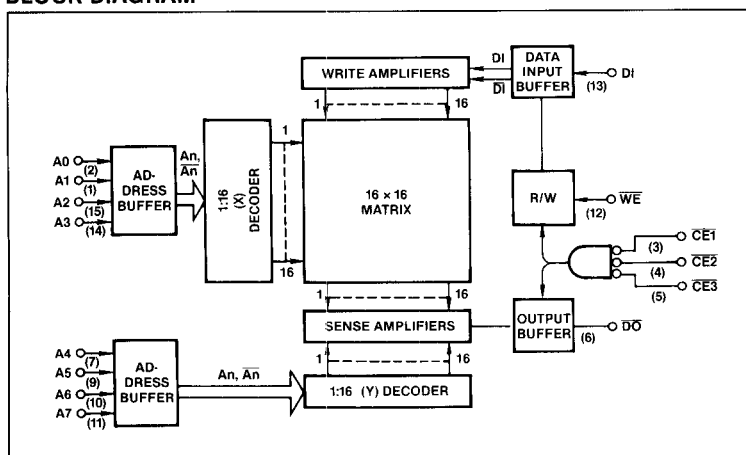
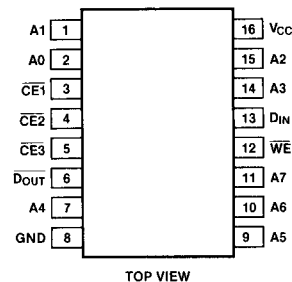
- Power dissipation: 0.98mW/bit typ
- Input loading:
N74LS301: – 100 μ A max
S54LS301: – 250 μ A max
- Output blanking during Write
- On-chip address decoding
- Schottky clamped
- TTL compatible

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

ABSOLUTE MAXIMUM RATINGS

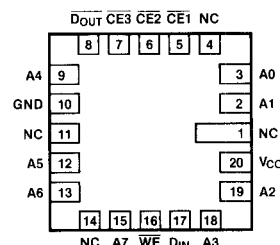
PARAMETER	RATING	UNIT
V_{CC} Supply voltage	+ 7	Vdc
V_{IN} Input voltage	+ 5.5	Vdc
V_{OUT} Output voltage	+ 5.5	Vdc
Temperature Range		
T_A Operating	0 to + 70	°C
N grade	– 55 to + 125	
S grade		
T_{STG} Storage	– 65 to + 150	°C

BLOCK DIAGRAM**PIN CONFIGURATIONS****F, N, W PACKAGE**

TOP VIEW

Order Numbers:

F = Cerdip N74LS301F or N74LS301N
N = Plastic S54LS301F or S54LS301W
W = Flat Pak

G PACKAGE

TOP VIEW

Order Number:
S54LS301G

G = Leadless

256-BIT TTL RAM (256 × 1)**54/74LS301 (O.C.)**

DC ELECTRICAL CHARACTERISTICS N74LS301: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S54LS301: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS	N74LS301			S54LS301			UNIT
		Min	Typ ¹	Max	Min	Typ ¹	Max	
V_{IL} V_{IH} V_{IC}	Input voltage ² Low High Clamp ³ $V_{CC} = \min$ $V_{CC} = \max$ $V_{CC} = \min$, $I_{IN} = -18\text{mA}$	2.0		0.85 -1.2	2.0		0.8 -1.2	V
V_{OL}	Output voltage Low ⁵ $V_{CC} = \min$ $I_{OL} = 16\text{mA}$			0.45			0.50	V
I_{IL} I_{IH}	Input current ² Low High $V_{CC} = \max$ $V_{IL} = 0.45\text{V}$ $V_{IH} = 2.7\text{V}$			-100 25			-250 25	μA
I_{OLK}	Output current Leakage ⁵ $V_{IH} = 2\text{V}$, $V_O = 5.5\text{V}$			40			50	μA
I_{CC}	V_{CC} supply current ⁸ $V_{CC} = \max$		50	70		50	100	mA
C_{IN} C_{OUT}	Capacitance Input Output $V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 1\text{K}\Omega$, $C_L = 15\text{pF}$
 N74LS301: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S54LS301: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N74LS301			S54LS301			UNIT
			Min	Typ ¹	Max	Min	Typ ¹	Max	
T_{AA} T_{CE}	Access time Address Chip enable Output Output	Address Chip enable		30 15	40 25		30 15	70 40	ns
T_{CD} T_{WD}	Disable time Valid time Output Output	Chip enable Write enable		15 30	25 40		15 30	40 55	ns ns
T_{WSA} T_{WHA} T_{WSD} T_{WHD} T_{WSC} T_{WHC}	Setup and hold time Setup time Hold time Setup time Hold time Setup time Hold time	Write enable Address Write enable Data in Write enable $\overline{CE}$	0 0 25 0 0 0	-5 -5 15 -5 -5 -5		10 10 40 10 10 10	-5 -5 15 -5 -5 -5		ns
T_{WP}	Pulse width Write enable ⁹		25	15		40	15		ns

NOTES

- All typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^{\circ}\text{C}$.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic low stored and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
- Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
- Duration of the short-circuit should not exceed 1 second.
- I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.

256-BIT TTL RAM (256 × 1)

54/74LS301 (O.C.)

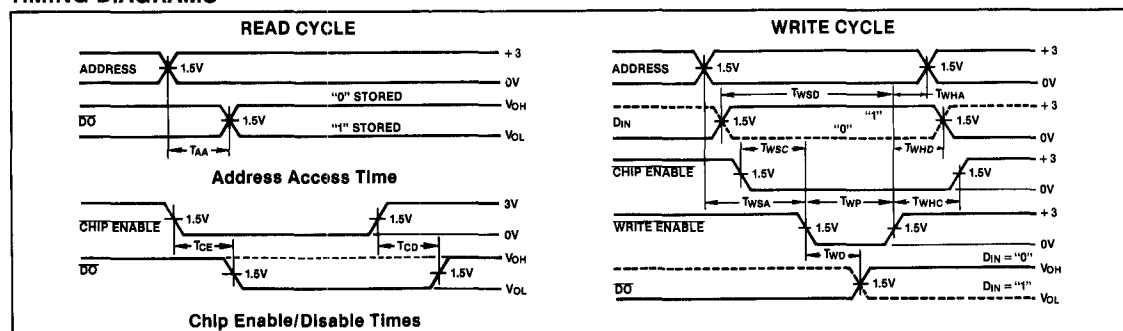
TRUTH TABLE

MODE	$\overline{CE}^*$	$\overline{WE}$	D_{IN}	D_{OUT}		
				54/74S301, 54/74LS301	82S16/LS16	82S17/LS17
Read	0	1	X	Stored data	Stored data	Stored data
Write "0"	0	0	0	1	1	1
Write "1"	0	0	1	1	0	0
Disabled	1	X	X	1	Hi-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.

X = Don't care.

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of chip enable low (with address valid) and when data output becomes valid.

T_{CD} Delay between when chip enable becomes high and data output is in off state.

T_{AA} Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

T_{WSC} Required delay between beginning of valid chip enable and beginning of Write enable pulse.

T_{WHD} Required delay between end of Write enable pulse and end of valid input data.

T_{WP} Width of Write enable pulse.

T_{WSA} Required delay between beginning of valid address and beginning of Write enable pulse.

T_{WSD} Required delay between beginning of valid data input and end of Write enable pulse.

T_{WD} Delay between beginning of Write enable pulse and when data output reflects complement of data input.

T_{WHC} Required delay between end of Write enable pulse and end of chip enable.

T_{WHA} Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT AND VOLTAGE WAVEFORM

