## 14A, 600V, UFS Series N-Channel IGBTs

The HGTD7N60B3S, HGT1S7N60B3S and HGTP7N60B3 are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between $25^{\circ} \mathrm{C}$ and $150^{\circ} \mathrm{C}$.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.
Formerly Developmental Type TA49190.

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
| :--- | :--- | :--- |
| HGTD7N60B3S | TO-252AA | G7N60B |
| HGT1S7N60B3S | TO-263AB | G7N60B3 |
| HGTP7N60B3 | TO-220AB | G7N60B3 |

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA and TO-263AB variant in tape and reel, e.g., HGTD7N60B3S9A.

## Symbol



## Features

- $14 \mathrm{~A}, 600 \mathrm{~V}, \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$
- 600 V Switching SOA Capability
- Typical Fall Time. . . . . . . . . . . . . . . . . 120 ns at $\mathrm{T}_{\mathrm{J}}=150^{\circ} \mathrm{C}$
- Short Circuit Rating
- Low Conduction Loss


## Packaging

JEDEC TO-220AB


JEDEC TO-263AB


JEDEC TO-252AA


INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

| $4,364,073$ | $4,417,385$ | $4,430,792$ | $4,443,931$ | $4,466,176$ | $4,516,143$ | $4,532,534$ | $4,587,713$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $4,598,461$ | $4,605,948$ | $4,620,211$ | $4,631,564$ | $4,639,754$ | $4,639,762$ | $4,641,162$ | $4,644,637$ |
| $4,682,195$ | $4,684,413$ | $4,694,313$ | $4,717,679$ | $4,743,952$ | $4,783,690$ | $4,794,432$ | $4,801,986$ |
| $4,803,533$ | $4,809,045$ | $4,809,047$ | $4,810,665$ | $4,823,176$ | $4,837,606$ | $4,860,080$ | $4,883,767$ |
| $4,888,627$ | $4,890,143$ | $4,901,127$ | $4,904,609$ | $4,933,740$ | $4,963,951$ | $4,969,027$ |  |

Absolute Maximum Ratings $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, Unless Otherwise Specified

|  |  | ALL TYPES | UNITS |
| :---: | :---: | :---: | :---: |
| Collector to Emitter Voltage | $\mathrm{BV}_{\text {CES }}$ | 600 | V |
| Collector Current Continuous |  |  |  |
| At $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | . . ${ }_{\text {C25 }}$ | 14 | A |
| At $\mathrm{T}_{\mathrm{C}}=110^{\circ} \mathrm{C}$ | . . ${ }_{\text {C110 }}$ | 7 | A |
| Collector Current Pulsed (Note 1) | . ${ }^{\text {ICM }}$ | 56 | A |
| Gate to Emitter Voltage Continuous. | . $\mathrm{V}_{\mathrm{GES}}$ | $\pm 20$ | V |
| Gate to Emitter Voltage Pulsed | $V_{\text {GEM }}$ | $\pm 30$ | V |
| Switching Safe Operating Area at $\mathrm{T}_{J}=150^{\circ} \mathrm{C}$, Figure 2 | SSOA | 35 A at 600 V |  |
| Power Dissipation Total at $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | $\ldots \mathrm{P}_{\mathrm{D}}$ | 60 | W |
| Power Dissipation Derating $\mathrm{T}_{\mathrm{C}}>25^{\circ} \mathrm{C}$ |  | 0.476 | W/ ${ }^{\circ} \mathrm{C}$ |
| Reverse Voltage Avalanche Energy. | . EARV | 100 | mJ |
| Operating and Storage Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}, \mathrm{T}_{\text {STG }}$ | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Lead Temperature for Soldering | $\ldots . .{ }_{\text {L }}$ | 260 | ${ }^{\circ} \mathrm{C}$ |
| Short Circuit Withstand Time (Note 2) at $\mathrm{V}_{\mathrm{GE}}=15 \mathrm{~V}$. | . . . ${ }_{\text {tsc }}$ | 2 | $\mu \mathrm{s}$ |
| Short Circuit Withstand Time (Note 2) at $\mathrm{V}_{\mathrm{GE}}=10 \mathrm{~V}$. | . . .tsc | 12 | $\mu \mathrm{s}$ |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTES:

1. Single Pulse; Pulse width limited by maximum junction temperature. Parts may current limit at less than $\mathrm{I}_{\mathrm{CM}}$ -
2. $\mathrm{V}_{\mathrm{CE}}=360 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=125^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{G}}=50 \Omega$.

Electrical Specifications $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Collector to Emitter Breakdown Voltage | $\mathrm{BV}_{\text {CES }}$ | $\mathrm{I}_{\mathrm{C}}=250 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{GE}}=0 \mathrm{~V}$ |  | 600 | - | - | V |
| Emitter to Collector Breakdown Voltage | BVECS | $\mathrm{IC}=3 \mathrm{~mA}, \mathrm{~V}_{\mathrm{GE}}=0 \mathrm{~V}$ |  | 15 | 28 | - | V |
| Collector to Emitter Leakage Current | ICES | $\mathrm{V}_{\text {CE }}=B \mathrm{~V}_{\text {CES }}$ | $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | - | - | 100 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\mathrm{C}}=150^{\circ} \mathrm{C}$ | - | - | 2.0 | mA |
| Collector to Emitter Saturation Voltage | $\mathrm{V}_{\text {CE(SAT }}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{C}}=\mathrm{I}_{\mathrm{C} 110}, \\ & \mathrm{~V}_{\mathrm{GE}}=15 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | - | 1.8 | 2.1 | V |
|  |  |  | $\mathrm{T}_{\mathrm{C}}=150^{\circ} \mathrm{C}$ | - | 2.1 | 2.4 | V |
| Gate to Emitter Threshold Voltage | $\mathrm{V}_{\mathrm{GE} \text { (TH) }}$ | $\mathrm{I}_{\mathrm{C}}=250 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{GE}}$ |  | 3.0 | 5.1 | 6.0 | V |
| Gate to Emitter Leakage Current | $\mathrm{I}_{\text {GES }}$ | $\mathrm{V}_{\mathrm{GE}}= \pm 20 \mathrm{~V}$ |  | - | - | $\pm 100$ | nA |
| Switching SOA | SSOA | $\begin{aligned} & \hline \mathrm{T}_{J}=150^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{G}}=50 \Omega \\ & \mathrm{~V}_{\mathrm{GE}}=15 \mathrm{~V} \\ & \mathrm{~L}=100 \mu \mathrm{H} \end{aligned}$ | $\mathrm{V}_{\text {CE }}=480 \mathrm{~V}$ | 42 | - | - | A |
|  |  |  | $\mathrm{V}_{\mathrm{CE}}=600 \mathrm{~V}$ | 35 | - | - | A |
| Gate to Emitter Plateau Voltage | $\mathrm{V}_{\mathrm{GEP}}$ | $\mathrm{I}_{\mathrm{C}}=\mathrm{I}_{\mathrm{C} 110}, \mathrm{~V}_{\text {CE }}=0.5 \mathrm{BV}_{\text {CES }}$ |  | - | 7.7 | - | V |
| On-State Gate Charge | $\mathrm{Q}_{\mathrm{G}(\mathrm{ON})}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{C}}=\mathrm{I}_{\mathrm{C} 110}, \\ & \mathrm{~V}_{\mathrm{CE}}=0.5 \mathrm{BV} \end{aligned}$ | $\mathrm{V}_{\mathrm{GE}}=15 \mathrm{~V}$ | - | 23 | 28 | nc |
|  |  |  | $\mathrm{V}_{\mathrm{GE}}=20 \mathrm{~V}$ | - | 30 | 37 | nC |
| Current Turn-On Delay Time | $\mathrm{t}_{\mathrm{d}(\mathrm{ON}) \mathrm{l}}$ | $\begin{aligned} & \text { IGBT and Diode Both at } \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{I}_{\mathrm{CE}}=\mathrm{I}_{\mathrm{C} 110}, \mathrm{~V}_{\mathrm{CE}}=0.8 \mathrm{BV} \mathrm{CES}, \\ & \mathrm{~V}_{\mathrm{GE}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{G}}=50 \Omega, \mathrm{~L}=2 \mathrm{mH} \\ & \text { Test Circuit (Figure 17) } \end{aligned}$ |  | - | 26 | - | ns |
| Current Rise Time | $\mathrm{trl}_{\mathrm{rl}}$ |  |  | - | 21 | - | ns |
| Current Turn-Off Delay Time | $\mathrm{t}_{\mathrm{d} \text { (OFF) }}$ |  |  | - | 130 | 160 | ns |
| Current Fall Time | $\mathrm{t}_{\mathrm{fl}}$ |  |  | - | 60 | 80 | ns |
| Turn-On Energy (Note 4) | EON1 |  |  | - | 72 | - | $\mu \mathrm{J}$ |
| Turn-On Energy (Note 4) | EON2 |  |  | - | 160 | 200 | $\mu \mathrm{J}$ |
| Turn-Off Energy (Note 3) | EOFF |  |  | - | 120 | 200 | $\mu \mathrm{J}$ |

## Electrical Specifications $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, Unless Otherwise Specified (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Current Turn-On Delay Time | $\mathrm{t}_{\mathrm{d}(\mathrm{ON}) \mathrm{I}}$ | IGBT and Diode Both at $\mathrm{T}_{\mathrm{J}}=150^{\circ} \mathrm{C}$ <br> $\mathrm{I}_{\mathrm{CE}}=\mathrm{I}_{\mathrm{C} 110}, \mathrm{~V}_{\mathrm{CE}}=0.8 \mathrm{BV}_{\text {CES }}$, <br> $\mathrm{V}_{\mathrm{GE}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{G}}=50 \Omega, \mathrm{~L}=2 \mathrm{mH}$ <br> Test Circuit (Figure 17) | - | 24 | - | ns |
| Current Rise Time | $\mathrm{trl}_{\mathrm{rl}}$ |  | - | 22 | - | ns |
| Current Turn-Off Delay Time | $\mathrm{t}_{\mathrm{d} \text { (OFF) }}$ |  | - | 230 | 295 | ns |
| Current Fall Time | $\mathrm{t}_{\mathrm{fl}}$ |  | - | 120 | 175 | ns |
| Turn-On Energy (Note 4) | EON1 |  | - | 80 | - | $\mu \mathrm{J}$ |
| Turn-On Energy (Note 4) | EON2 |  | - | 310 | 350 | $\mu \mathrm{J}$ |
| Turn-Off Energy (Note 3) | EOFF |  | - | 350 | 500 | $\mu \mathrm{J}$ |
| Thermal Resistance Junction To Case | $\mathrm{R}_{\text {өJC }}$ |  | - | - | 2.1 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTE:
3. Turn-Off Energy Loss (EOFF) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (ICE = OA). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include losses due to diode recovery.
4. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. EON 1 is the Turn-On loss of the IGBT only. EON2 is the Turn-On loss when a typical diode is used in the test circuit and the diode is at the same $T_{J}$ as the IGBT. The diode type is specified in Figure 17.

Typical Performance Curves Unless Otherwise Specified


FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

## Typical Performance Curves Unless Otherwise Specified (Continued)



FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT


FIGURE 5. COLLECTOR TO EMITTER ON STATE VOLTAGE


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME


FIGURE 6. COLLECTOR TO EMITTER ON STATE VOLTAGE


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT


FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

$\mathrm{V}_{\mathrm{GE}}$, GATE TO EMITTER VOLTAGE (V)
FIGURE 13. TRANSFER CHARACTERISTIC


FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT


FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT


FIGURE 14. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified (Continued)


FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE


FIGURE 16. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

## Test Circuit and Waveforms



FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT


FIGURE 18. SWITCHING TEST WAVEFORMS

## Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBDTM LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating - Never exceed the gate-voltage rating of $\mathrm{V}_{\mathrm{GEM}}$. Exceeding the rated $\mathrm{V}_{\mathrm{GE}}$ can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. Gate Protection - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

## Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ( ${ }^{\text {CE }}$ ) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows $f_{M A X 1}$ or $f_{M A X 2}$; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.
$f_{M A X 1}$ is defined by $f_{M A X 1}=0.05 /\left(t_{d(O F F) I}+t_{d(O N) I}\right)$. Deadtime (the denominator) has been arbitrarily held to 10\% of the on-state time for a $50 \%$ duty factor. Other definitions are possible. $\mathrm{t}_{\mathrm{d}(\mathrm{OFF}) \mid}$ and $\mathrm{t}_{\mathrm{d}(\mathrm{ON}) \mid}$ are defined in Figure 18. Device turn-off delay can establish an additional frequency limiting condition for an application other than $\left.\mathrm{T}_{\mathrm{JM}} \cdot \mathrm{t}_{\mathrm{d}(\mathrm{OFF})}\right)$ is important when controlling output ripple under a lightly loaded condition.
$f_{\text {MAX2 }}$ is defined by $f_{\text {MAX2 }}=\left(P_{D}-P_{C}\right) /\left(E_{O F F}+E_{O N 2}\right)$. The allowable dissipation ( $P_{D}$ ) is defined by $P_{D}=\left(T_{J M}-T_{C}\right) / R_{\theta J C}$. The sum of device switching and conduction losses must not exceed $P_{D}$. A 50\% duty factor was used (Figure 3) and the conduction losses ( $\mathrm{P}_{\mathrm{C}}$ ) are approximated by $\mathrm{P}_{\mathrm{C}}=\left(\mathrm{V}_{\mathrm{CE}} \times \mathrm{I}_{\mathrm{CE}}\right) / 2$.
$\mathrm{E}_{\mathrm{ON} 2}$ and $\mathrm{E}_{\mathrm{OFF}}$ are defined in the switching waveforms shown in Figure 18. $\mathrm{E}_{\mathrm{ON} 2}$ is the integral of the instantaneous power loss ( $\mathrm{I}_{\mathrm{CE}} \times \mathrm{V}_{\mathrm{CE}}$ ) during turn-on and $\mathrm{E}_{\mathrm{OFF}}$ is the integral of the instantaneous power loss ( $l_{C E} \times \mathrm{V}_{\mathrm{CE}}$ ) during turn-off. All tail losses are included in the calculation for E i.e., the collector current equals zero ( $\mathrm{I} C E=0$ ).

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

