

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF40194B

### MSI

## 4-bit bidirectional universal shift register

Product specification  
File under Integrated Circuits, IC04

January 1995

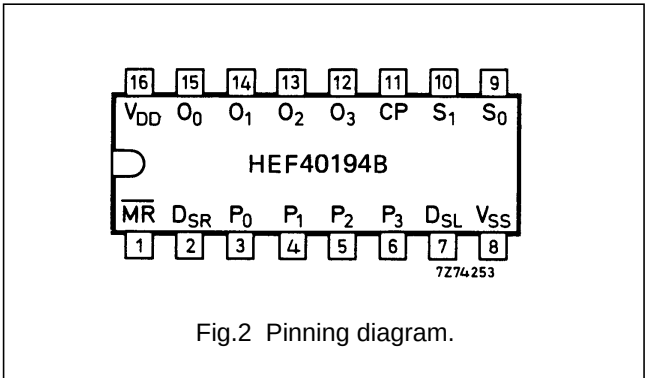
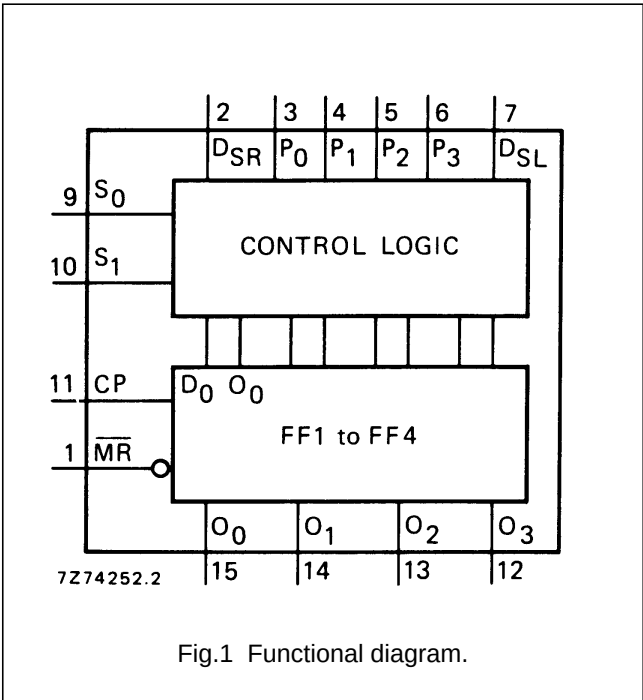
4-bit bidirectional universal shift register

HEF40194B  
MSI

DESCRIPTION

The HEF40194B is a 4-bit bidirectional shift register with two mode control inputs ( $S_0$  and  $S_1$ ), a clock input (CP), a serial data shift left input ( $D_{SL}$ ), a serial data shift right input ( $D_{SR}$ ), four parallel data inputs ( $P_0$  to  $P_3$ ), an overriding asynchronous master reset input ( $\overline{MR}$ ), and four buffered parallel outputs ( $O_0$  to  $O_3$ ). When LOW,  $\overline{MR}$  resets all stages and forces  $O_0$  to  $O_3$  LOW, overriding all other input conditions. When  $\overline{MR}$  is HIGH, the operation mode is controlled by  $S_0$  and  $S_1$  as shown in the function table.

Serial and parallel operation are edge-triggered on the LOW to HIGH transition of CP. The inputs at which the data are to be entered and  $S_0$ ,  $S_1$  must be stable for a set-up time before the LOW to HIGH transition of CP.



PINNING

- $S_0$ ,  $S_1$  mode control inputs
- $P_0$  to  $P_3$  parallel data inputs
- $D_{SR}$  serial data shift right input
- $D_{SL}$  serial data shift left input
- CP clock input (LOW to HIGH edge-triggered)
- $\overline{MR}$  master reset input (active LOW)
- $O_0$  to  $O_3$  buffered parallel outputs

FAMILY DATA,  $I_{DD}$  LIMITS category MSI

See Family Specifications

4-bit bidirectional universal shift register

HEF40194B  
MSI

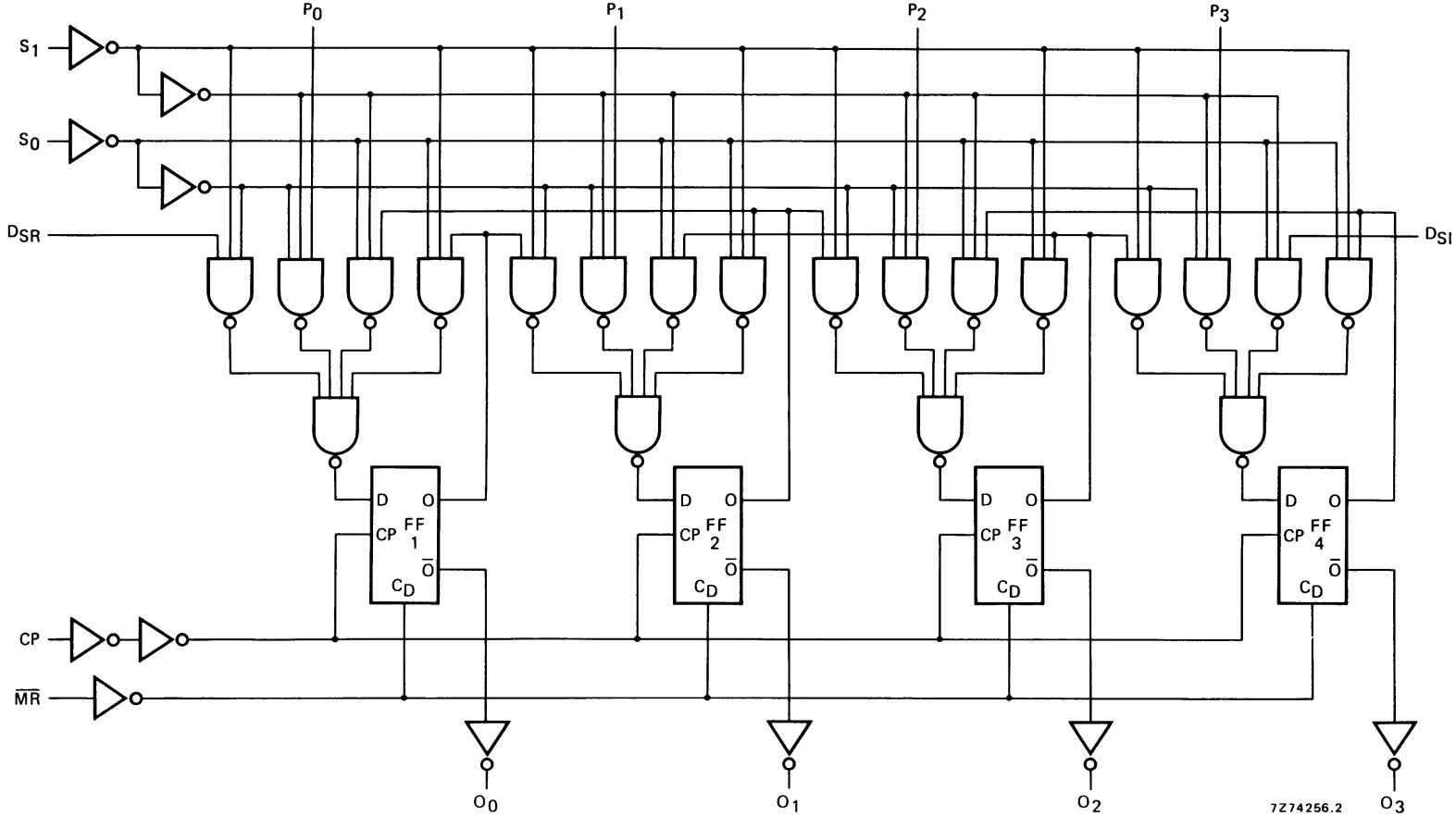


Fig.3 Logic diagram.

## 4-bit bidirectional universal shift register

HEF40194B  
MSI

## FUNCTION TABLE

| OPERATING MODE | INPUTS ( $\overline{MR} = \text{HIGH}$ ) |       |          |          |                | OUTPUTS AT $T_{n+1}$ |       |       |       |
|----------------|------------------------------------------|-------|----------|----------|----------------|----------------------|-------|-------|-------|
|                | $S_1$                                    | $S_0$ | $D_{SR}$ | $D_{SL}$ | $P_0$ TO $P_3$ | $O_0$                | $O_1$ | $O_2$ | $O_3$ |
| hold           | L                                        | L     | X        | X        | X              | $O_0$                | $O_1$ | $O_2$ | $O_3$ |
| shift left     | H                                        | L     | X        | L        | X              | $O_1$                | $O_2$ | $O_3$ | L     |
|                | H                                        | L     | X        | H        | X              | $O_1$                | $O_2$ | $O_3$ | H     |
| shift right    | L                                        | H     | L        | X        | X              | L                    | $O_0$ | $O_1$ | $O_2$ |
|                | L                                        | H     | H        | X        | X              | H                    | $O_0$ | $O_1$ | $O_2$ |
| parallel load  | H                                        | H     | X        | X        | L              | L                    | L     | L     | L     |
|                | H                                        | H     | X        | X        | H              | H                    | H     | H     | H     |

## Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4.  $t_{n+1}$  = state after next LOW to HIGH transition of CP

## AC CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; input transition times  $\leq 20 \text{ ns}$ 

|                                           | $V_{DD}$<br>V | TYPICAL FORMULA FOR P ( $\mu\text{W}$ )                                                                                                          |                                                                                                                                                                  |
|-------------------------------------------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Dynamic power dissipation per package (P) | 5<br>10<br>15 | $1\,500 f_i + \sum (f_o C_L) \times V_{DD}^2$<br>$6\,900 f_i + \sum (f_o C_L) \times V_{DD}^2$<br>$18\,900 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where<br>$f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load cap. (pF)<br>$\sum (f_o C_L)$ = sum of outputs<br>$V_{DD}$ = supply voltage (V) |

## 4-bit bidirectional universal shift register

HEF40194B  
MSI

## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

|                                               | V <sub>DD</sub><br>V | SYMBOL           | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION<br>FORMULA |                                     |
|-----------------------------------------------|----------------------|------------------|------|------|------|----------------------------------|-------------------------------------|
| Propagation delays                            |                      |                  |      |      |      |                                  |                                     |
| CP → O <sub>n</sub>                           | 5                    |                  |      | 100  | 205  | ns                               | 73 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                                   | 10                   | t <sub>PHL</sub> |      | 40   | 85   | ns                               | 29 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                               | 15                   |                  |      | 30   | 60   | ns                               | 22 ns + (0,16 ns/pF) C <sub>L</sub> |
| LOW to HIGH                                   | 5                    |                  |      | 80   | 165  | ns                               | 53 ns + (0,55 ns/pF) C <sub>L</sub> |
|                                               | 10                   | t <sub>PLH</sub> |      | 35   | 70   | ns                               | 24 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                               | 15                   |                  |      | 25   | 55   | ns                               | 17 ns + (0,16 ns/pF) C <sub>L</sub> |
| $\overline{\text{MR}} \rightarrow \text{O}_n$ | 5                    |                  |      | 85   | 175  | ns                               | 58 ns + (0,55 ns/pF) C <sub>L</sub> |
| HIGH to LOW                                   | 10                   | t <sub>PHL</sub> |      | 40   | 80   | ns                               | 29 ns + (0,23 ns/pF) C <sub>L</sub> |
|                                               | 15                   |                  |      | 30   | 60   | ns                               | 22 ns + (0,16 ns/pF) C <sub>L</sub> |
| Output transition times                       | 5                    |                  |      | 60   | 120  | ns                               | 10 ns + (1,0 ns/pF) C <sub>L</sub>  |
| HIGH to LOW                                   | 10                   | t <sub>THL</sub> |      | 30   | 60   | ns                               | 9 ns + (0,42 ns/pF) C <sub>L</sub>  |
|                                               | 15                   |                  |      | 20   | 40   | ns                               | 6 ns + (0,28 ns/pF) C <sub>L</sub>  |
| LOW to HIGH                                   | 5                    |                  |      | 60   | 120  | ns                               | 10 ns + (1,0 ns/pF) C <sub>L</sub>  |
|                                               | 10                   | t <sub>TLH</sub> |      | 30   | 60   | ns                               | 9 ns + (0,42 ns/pF) C <sub>L</sub>  |
|                                               | 15                   |                  |      | 20   | 40   | ns                               | 6 ns + (0,28 ns/pF) C <sub>L</sub>  |

## 4-bit bidirectional universal shift register

HEF40194B  
MSI

|                                                         | V <sub>DD</sub><br>V | SYMBOL            | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION<br>FORMULA   |
|---------------------------------------------------------|----------------------|-------------------|------|------|------|------------------------------------|
| Set-up times                                            | 5                    |                   | 80   | 40   | ns   | see also waveforms<br>Figs 4 and 5 |
| P <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> → CP | 10                   | t <sub>su</sub>   | 30   | 15   | ns   |                                    |
|                                                         | 15                   |                   | 20   | 10   | ns   |                                    |
| S <sub>n</sub> → CP                                     | 5                    |                   | 140  | 70   | ns   |                                    |
|                                                         | 10                   | t <sub>su</sub>   | 60   | 30   | ns   |                                    |
|                                                         | 15                   |                   | 40   | 20   | ns   |                                    |
| Hold times                                              | 5                    |                   | 10   | −30  | ns   |                                    |
| P <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> → CP | 10                   | t <sub>hold</sub> | 5    | −10  | ns   |                                    |
|                                                         | 15                   |                   | 5    | −5   | ns   |                                    |
| S <sub>n</sub> → CP                                     | 5                    |                   | 25   | −45  | ns   |                                    |
|                                                         | 10                   | t <sub>hold</sub> | 15   | −15  | ns   |                                    |
|                                                         | 15                   |                   | 10   | −10  | ns   |                                    |
| Minimum clock<br>pulse width; LOW                       | 5                    |                   | 50   | 25   | ns   |                                    |
|                                                         | 10                   | t <sub>WCPL</sub> | 20   | 10   | ns   |                                    |
|                                                         | 15                   |                   | 20   | 10   | ns   |                                    |
| Minimum $\overline{\text{MR}}$<br>pulse width; LOW      | 5                    |                   | 80   | 40   | ns   |                                    |
|                                                         | 10                   | t <sub>WMRL</sub> | 40   | 20   | ns   |                                    |
|                                                         | 15                   |                   | 30   | 15   | ns   |                                    |
| Recovery time<br>for $\overline{\text{MR}}$             | 5                    |                   | 30   | 10   | ns   |                                    |
|                                                         | 10                   | t <sub>RMR</sub>  | 15   | 5    | ns   |                                    |
|                                                         | 15                   |                   | 15   | 5    | ns   |                                    |
| Maximum clock<br>pulse frequency                        | 5                    |                   | 6    | 12   | MHz  |                                    |
|                                                         | 10                   | f <sub>max</sub>  | 15   | 30   | MHz  |                                    |
|                                                         | 15                   |                   | 20   | 40   | MHz  |                                    |

# 4-bit bidirectional universal shift register

HEF40194B  
MSI

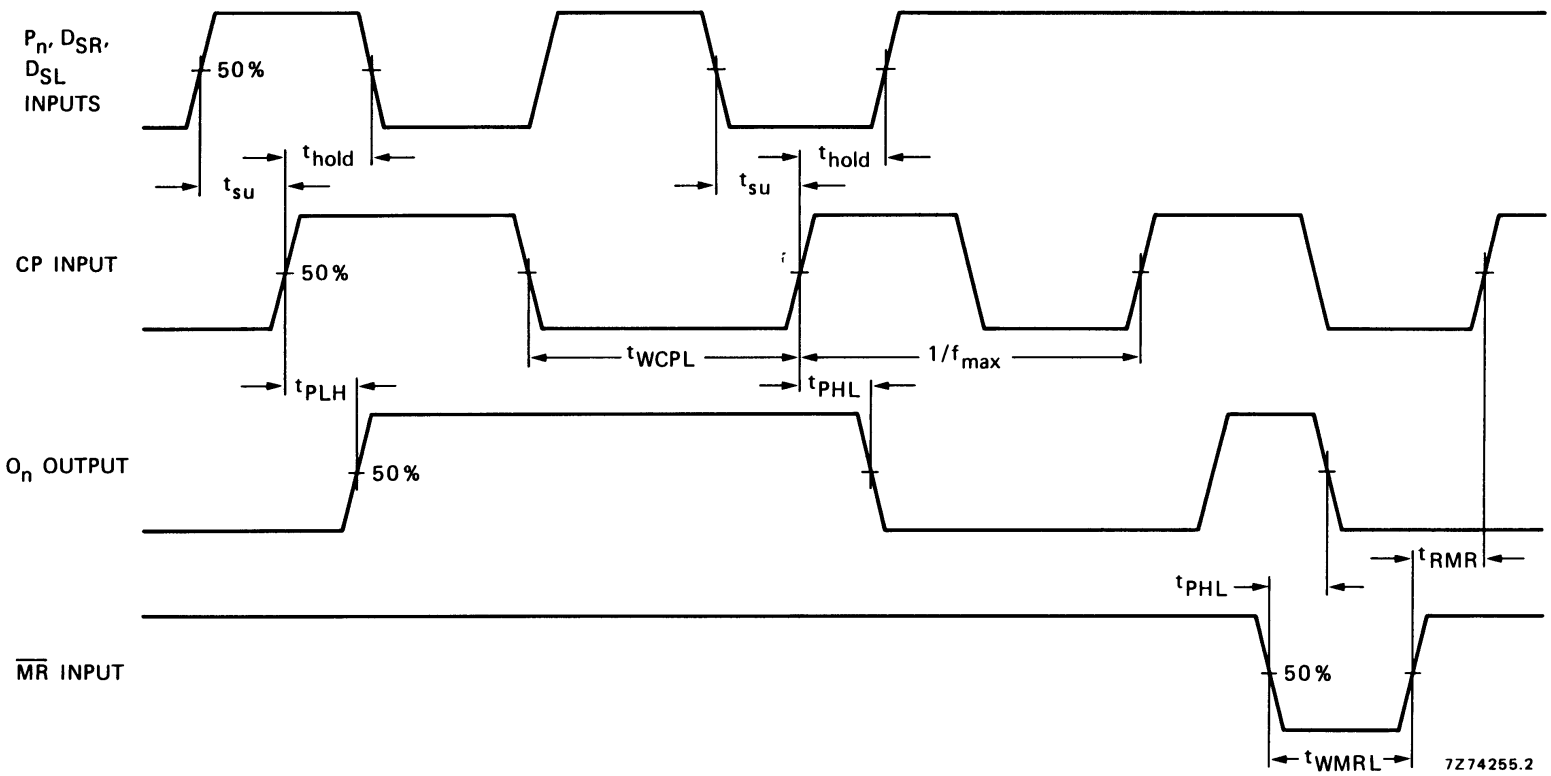


Fig.4 Waveforms showing set-up times, hold times for  $D_{SR}$ ,  $D_{SL}$  and  $P_n$  inputs; minimum  $\overline{MR}$  pulse width,  $\overline{MR}$  to output delays and  $\overline{MR}$  to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.

## 4-bit bidirectional universal shift register

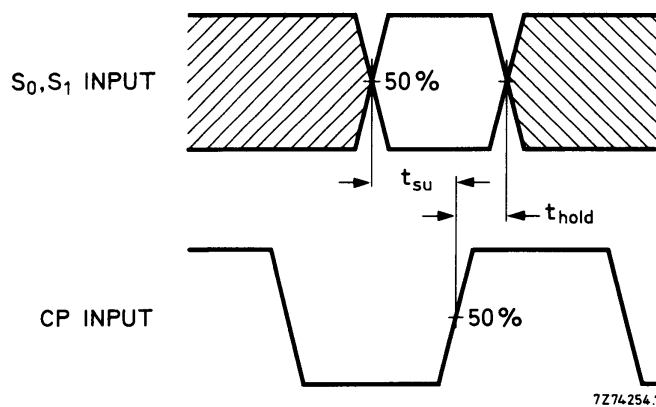
HEF40194B  
MSI

Fig.5 Waveforms showing set-up times and hold times for  $S_0$  and  $S_1$  inputs. Set-up and hold times are shown as positive values but may be specified as negative values.

**APPLICATION INFORMATION**

Some examples of applications for the HEF40194B are:

- Arithmetic unit register
- Serial/parallel converter.