

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4035B

MSI

4-bit universal shift register

Product specification
File under Integrated Circuits, IC04

January 1995

4-bit universal shift register

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DESCRIPTION

The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J , $\bar{K}$), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a true/complement input ($T/\bar{C}$) and an overriding asynchronous master reset input (MR). Each register is of a D-type master-slave flip-flop.

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and $\bar{K}$ and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and $\bar{K}$. When $J = \text{HIGH}$ and $\bar{K} = \text{LOW}$ the first stage is in the toggle mode. When $J = \text{LOW}$ and $\bar{K} = \text{HIGH}$ the first stage is in the hold mode.

The outputs (O_0 to O_3) are either inverting or non-inverting, depending on $T/\bar{C}$ state. With $T/\bar{C}$ HIGH, O_0 to O_3 are non-inverting (active HIGH) and when $T/\bar{C}$ is LOW, O_0 to O_3 are inverting (active LOW).

A HIGH on MR resets all four bit positions (O_0 to $O_3 = \text{LOW}$ if $T/\bar{C} = \text{HIGH}$, O_0 to $O_3 = \text{HIGH}$ if $T/\bar{C} = \text{LOW}$) independent of all other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

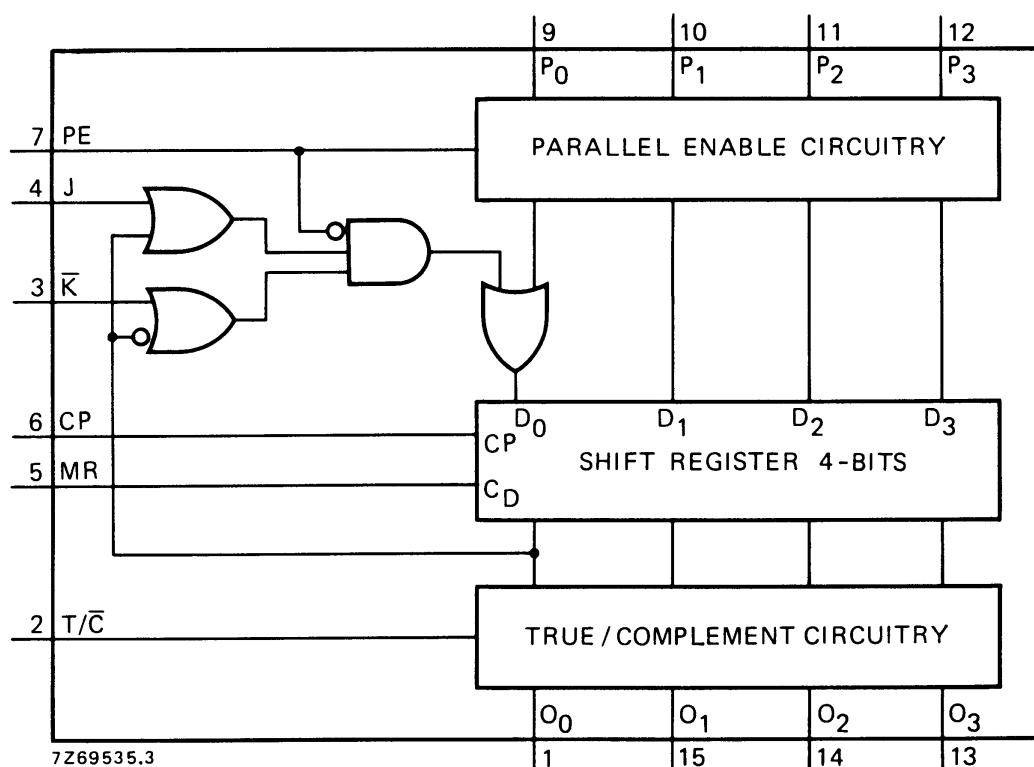


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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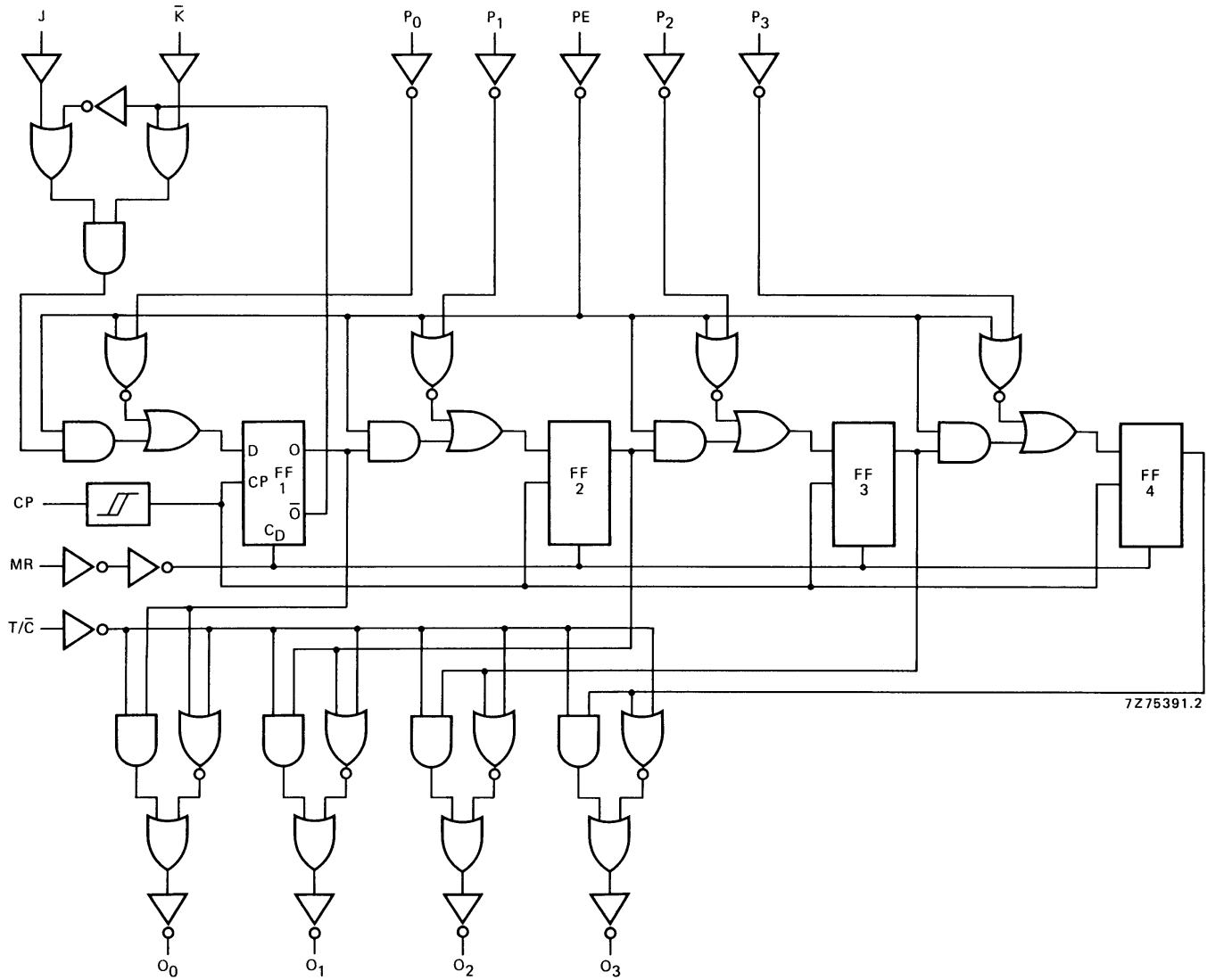
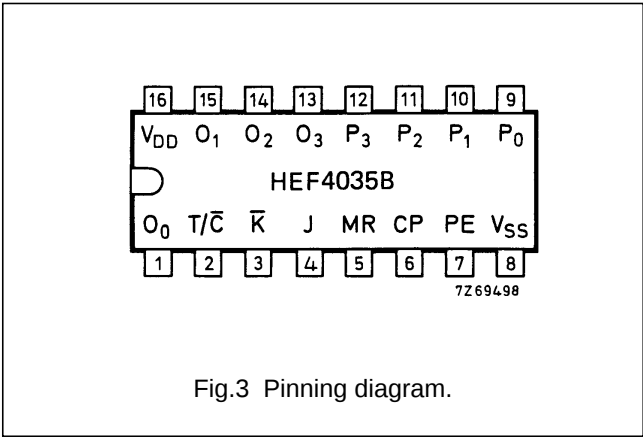


Fig.2 Logic diagram.

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- HEF4035BP(N): 16-lead DIL; plastic
(SOT38-1)
- HEF4035BD(F): 16-lead DIL; ceramic (cerdip)
(SOT74)
- HEF4035BT(D): 16-lead SO; plastic
(SOT109-1)
- (): Package Designator North America

PINNING

- PEparallel enable input
- P₀ to P₃parallel data inputs
- Jfirst stage J-input (active HIGH)
- K̄first stage K-input (active LOW)
- CPclock input (LOW to HIGH edge-triggered)
- T/C̄true/complement input
- MRmaster reset input
- O₀ to O₃buffered parallel outputs

FUNCTION TABLES

Serial operation first stage

INPUTS				OUTPUT	MODE OF OPERATION
CP	J	K̄	MR	O ₀₊₁	
	H	H	L	H	D flip-flop
	L	L	L	L	D flip-flop
	H	L	L	Ō ₀	toggle
	L	H	L	O ₀	no change
X	X	X	H	L	reset

Note

1. T/C̄ = HIGH; PE = LOW

Parallel operation

CP	INPUTS				OUTPUTS			
	P ₀	P ₁	P ₂	P ₃	O ₀	O ₁	O ₂	O ₃
	H	H	H	H	H	H	H	H
	L	L	L	L	L	L	L	L

Notes

1. T/C̄ = HIGH; PE = HIGH; MR = LOW
- = positive-going transition
- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
CP $\rightarrow$ O _n	5		170	340	ns	143 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}	70	140	ns	59 ns + (0,23 ns/pF) C _L
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	150	300	ns	123 ns + (0,55 ns/pF) C _L
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L
MR $\rightarrow$ O _n	5		115	230	ns	88 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	115	230	ns	88 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
T/ $\overline{C} \rightarrow$ O _n	5		105	210	ns	78 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	85	170	ns	58 ns + (0,55 ns/pF) C _L
	10		45	90	ns	34 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C _L
HIGH to LOW	10	t _{THL}	30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

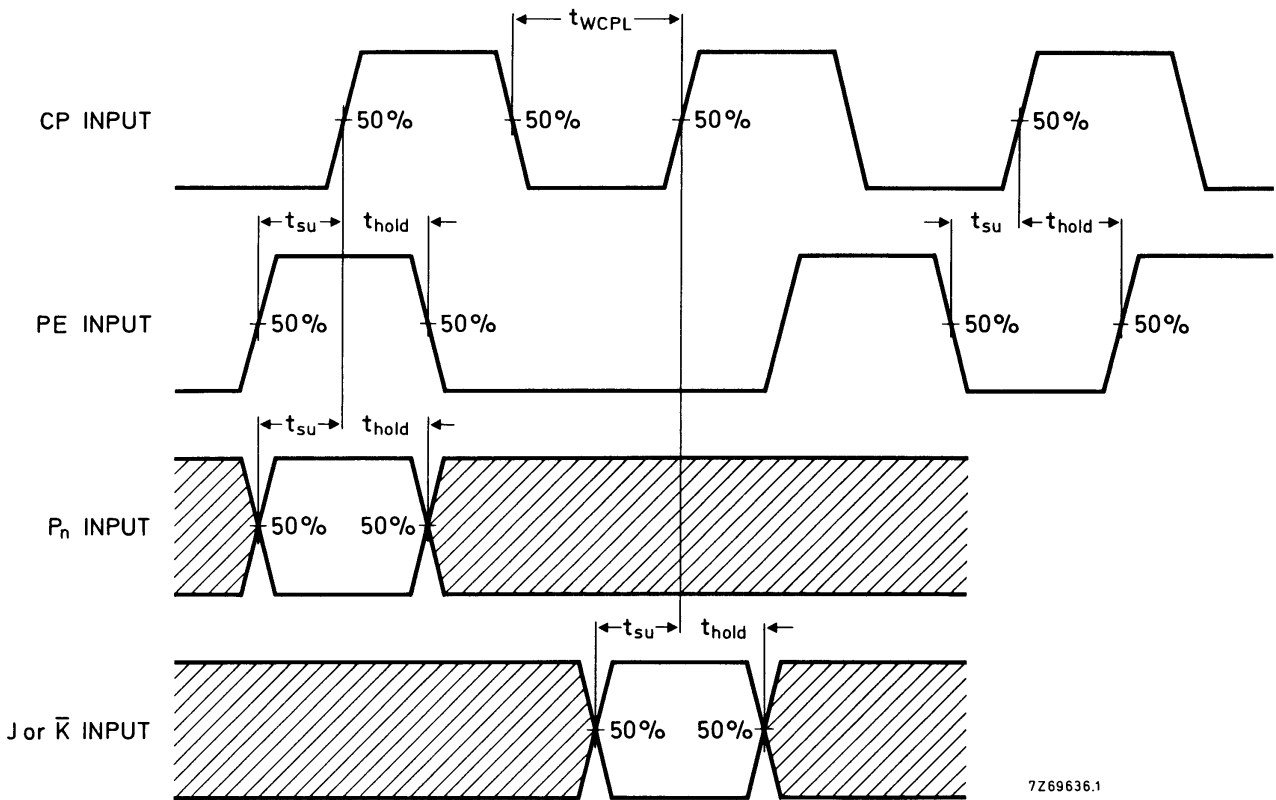
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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; LOW	5	t _{WCPL}	80	40	ns	see also waveforms Figs 4 and 5
	10		40	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t _{RMR}	50	20	ns	
	10		40	15	ns	
	15		25	10	ns	
Set-up times P _n → CP	5	t _{su}	40	5	ns	
	10		25	0	ns	
	15		15	0	ns	
PE → CP	5	t _{su}	50	25	ns	
	10		35	15	ns	
	15		30	10	ns	
J, $\bar{K}$ → CP	5	t _{su}	55	40	ns	
	10		35	15	ns	
	15		25	10	ns	
Hold times P _n → CP	5	t _{hold}	25	10	ns	
	10		20	10	ns	
	15		20	10	ns	
PE → CP	5	t _{hold}	15	−5	ns	
	10		10	−5	ns	
	15		5	−5	ns	
J, $\bar{K}$ → CP	5	t _{hold}	10	−5	ns	
	10		10	0	ns	
	15		10	0	ns	
Maximum clock pulse frequency	5	f _{max}	5	10	MHz	
	10		12	25	MHz	
	15		15	30	MHz	

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load cap. (pF) Σ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	$6\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$20\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

4-bit universal shift register

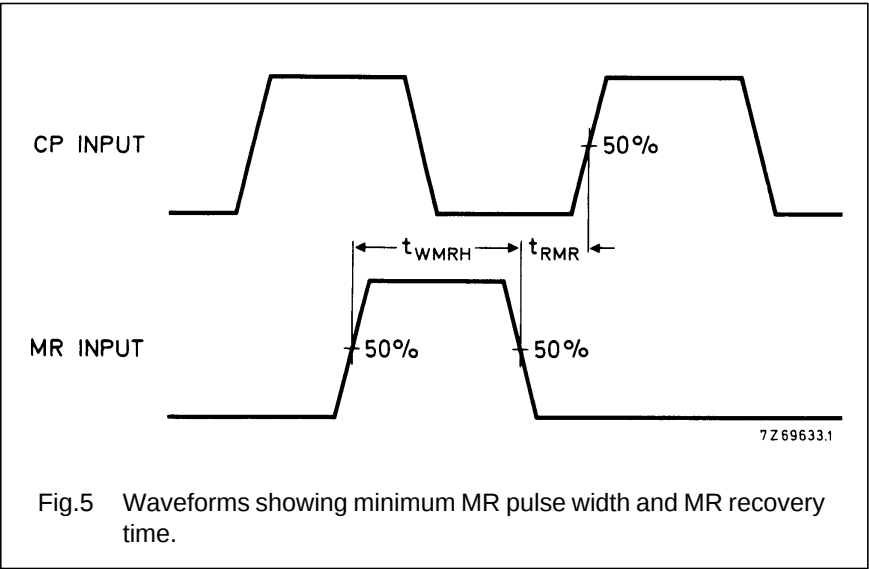
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Fig.4 Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

4-bit universal shift register

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APPLICATION INFORMATION

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- Control circuits.
- Code conversion.

